What is claimed is:

1. An integrated circuit testing apparatus, comprising:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit; and

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value.

2. An integrated circuit testing apparatus, comprising:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit; and

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

3. An integrated circuit testing apparatus, comprising:

a first test circuit operable to produce a first signal for determining at least one of an operating reference signal and a substrate coupling effect on a plurality of components within an integrated circuit; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

4. An integrated circuit testing apparatus, comprising:

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value; and

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components.

5. An integrated circuit testing apparatus, comprising:

a second test circuit operable to produce a second signal for determining at least one of a cross-talk effect on said plurality of components and the accuracy of an interconnect capacitance extraction value; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

6. An integrated circuit testing apparatus, comprising:

a third test circuit operable to produce a third signal for determining at least one of an effect of system noise on the operational speed of said plurality of components and a maximum degradation expected for a logic path between said plurality of components; and

a fourth test circuit operable to produce a fourth signal for determining an effect of power supply noise on a signal propagation delay within said plurality of components.

7. The apparatus of claims 1, 2, or 3 wherein said first test circuit further comprises a first ring oscillator, said first ring oscillator being routed to mimic a data path within said integrated circuit and being powered by an external power supply.

8. The apparatus of claims 1, 4, or 5 wherein said second test circuit further comprises a second ring oscillator, said second ring oscillator being routed within a core logic area of said integrated circuit and being powered by an external power supply.

9. The apparatus of claims 2 or 6 wherein said third test circuit further comprises a third ring oscillator, said third ring oscillator being randomly located within a core logic area of said integrated circuit and being powered by an external power supply.

10. The apparatus of claims 3 or 6 wherein said fourth test circuit further comprises a fourth ring oscillator, said fourth ring oscillator being routed to mimic a data path within said integrated circuit and sharing a power supply with a core logic area of said integrated circuit.